CP3000/3500AC54TE Global Platform Line High Efficiency Rectifier

Input: 100-120/220-277 Vac; Default Output: ±54 Vdc @ 3000W/3500W; 5 Vdc @ 10W

RoHS Compliant

Applications

- 48V_{DC} distributed power architectures
- Routers/ VoIP/Soft and other Telecom Switches
- LAN/WAN/MAN applications
- File servers, Enterprise Networks, Indoor wireless
- SAN/NAS/iSCSI applications

Targeted Countries

Argentina, Australia, Brazil, Canada, Chile, China, Dominican Republic, European Union, Guatemala, Indonesia, Israel, Japan, Laos, South Korea, Malaysia, Mexico, New Zealand, Philippines, Puerto Rico, Saudi Arabia, Singapore, Taiwan, Thailand, USA, Vietnam.

EU Countries

Potential countries: South America (those not yet listed), Africa

Features

- Efficiency meets 80plus Titanium requirements
- Compact 1RU form factor with 40 W/in^3 density
- Constant power from 52 – 58V_{DC}
- 3000 or 3500W from nominal 200-277V_{AC}
- 1500W from nominal 100 – 120V_{AC}
- Output voltage programmable from 42V – 58V_{DC}
- ON/OFF control of the main output
- Comprehensive input, output and overtemp. protection
- PMBus compliant dual I^{2}C serial bus and RS485
- Precision measurement reporting such as input power consumption, input/output voltage & current
- Remote firmware upgrade capable
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 2A Aux power
- Internally controlled Variable-speed fan
- Hot insertion/removal (hot plug)
- Four front panel LED indicators
- UL* Recognized to UL60950-1, CAN/ CSA† C22.2 No. 60950-1, and VDE‡ 0805-1 Licensed to IEC60950-1
- CE mark meets 2006/95/EC directive§

Description

The CP3000/3500AC54TEP Rectifiers provide significantly higher power density in the same form factor and efficiency improvements in the Compact Power Line of Rectifiers. The only difference between these rectifiers is output power limit. High-density front-to-back airflow is designed for minimal space utilization and is highly expandable for future growth. Wide-input enables the rectifier to be deployed internationally into a wide range of commercially available voltage sources. Configured with both dual-redundant I^{2}C and RS485 based communications busses, so that it could be positioned into a broad range of applications. Feature set flexibility makes this rectifier an excellent choice for applications requiring modular AC to - 48V_{DC} intermediate voltages, such as in distributed power.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.
† *CSA* is a registered trademark of Canadian Standards Association.
‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.
§ This product is intended for integration into end-user equipment. All *CE* marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)
** *ISO* is a registered trademark of the International Organization of Standards
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imagination at work

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Record of Changes

Revision	Description of Changes	Author	Date
1.0	Original release	Gabe Suranyi	May/05/2014
1.01	Added: Read_Status (0xD0h) should return the temperature reading of the sensor that is closest to shutdown. Added: PFW signal should pulse at a 1ms duty cycle when in overload Modified: Temperature sensor descriptions Deleted: OT_warn_limit and OT_fault_limit sensors Added: Restore_default_code into the command set Clarified: Vout_command can be used to change the firmware based default configuration. The Vprog pin is still used to override the firmware default configuration. Minor corrections made to harmonize changes within the document	Gabe Suranyi	May/16/2014
1.02	Current limit inception modified to add 3000W unit at a lower inception level Added FCI connector for backplane right angle mate w/AC line1 line2 wired I²C – Mfr_revision(0x9Bh) changed to product series number I²C - Read firmware rev(0xD5h) modified to be consistent with Galaxy I²C – Firmware update revised to be consistent with Galaxy protocol I²C – revised addressing algorithm I²C – Added Read_temp_exhaust (0xDAh) Changed the targeted countries list	Gabe Suranyi	June/13/2014
1.03	I²C – Command set table; Changed the Vout_OV_fault_response description to note that it is a read only register. The command description properly described the register as read only already. I²C – Command set table: Added the default Iout warning and fault levels at low-line operation I²C – Changed wording of Restore_default_all and Restore_default_code to indicate that the contents of these registers are being placed into operating memory I²C – Corrected Read_Bus _Status register code, should be (0xD7h) I²C – Corrected Take_over_bus_control register code, should be (0xD8h) I²C – Added duty cycle control as the default for fan speed control I²C – Added OT warning and limit registers for the dc-sec temp. sensor I²C – Added Status_fans_1_2 (0x81h) Added startup voltage level and tolerance: 85 ± 5V_{AC} Added turn_off voltage level and tolerance: 80 ± 5V_{AC} Added hysteresis between turn_ON and turn_OFF: 5$V_{AC,MIN}$ Changed Vin_OV_fault_limit to a read_only register Changed Vin_UV_fault_limit to a read_only register, default is 85V_{AC} Added input current measurement range and accuracy, modified output current measurement accuracy in the digital interface table Added current limit reductions above 280V_{AC} and below 45V_{DC} output In RS485 mode changed shelf_ID to a maximum of 10 shelves Changed the Mod_Present signal pin connection to Logic_GRD Added a 3rd Alarm register to include new shutdown capabilities	Gabe Suranyi	July/14/2014
1.04	Corrected Tyco right angle PWB mate part # - error on Tyco drawing	Gabe Suranyi	July/15/2014
1.05	I²C – Corrected the number of bytes being read back by read_status (0xD0) and the read_alarm_state (0xD2) in the commands table. I²C – Added that Alert#_0 should be asserted during start up to notify the master that a rectifier has been added on the bus. I²C – Changed STATUS2 bit 6 from 'will restart' to 'will restart – OC' I²C – Changed STATUS1 bit 7 from 'x' to 'will restart – OT'	Gabe Suranyi	July/31/2014

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1.05 (continues)	I²C – Changed ALARM3 bits 3 – 1 to 'x' – not used in CP3500 I²C – Noted that The OC_fault_limit value sets where overcurrent starts. The rectifier actually shuts down when the output voltage falls below the OC_LV_fault_limit setting. I²C – Added Iout_OC_LV_fault_limit (0x48) command as a read only setting where the rectifier actually shuts down for low output voltage. I²C – Deleted the Vout_OV_fault_response line from the table under Standard features. This line was in conflict with the same command in the command table. I²C – Added a paragraph under Standard Features entitled Status and Alarm registers. The note reaffirms that the operational state information in these registers is constantly updated. I²C – Changed Vout_UV_fault_response to read only. Cannot be set to a latched state. I²C – Changed Iout_OC warning and shutdown registers to be configurable only at high line. Low line OC warning is set at 29A and OC shutdown is set at 30A. These low-line overload settings cannot be read or changed. Added note that when V_O > 57V power derating starts at 50°C Added that address detection requires impedance between **Slot_ID** and **Vout(-).**		
1.06	I²C – Change Restore_default_code to Restore_user_all I²C – Fan read command 0xD3 changed to linear format readback I²C – Status-1 register bit 0 clarified – Output ON (ON=1) I²C – In Status_byte bit 6 is clarified as OUTPUT OFF I²C – Clarified the triggering definition of the Alert# signal. RS485 – Added the Bay_ID definition for RS485 mode rectifiers	Gabe Suranyi	Aug/07/2014
1.07	I²C – Corrected the ARA response description to agree with PMBus I²C – Changed a number of command names (Status_summary [0xD0], status_unit [0xd1], status_alarm [0xD2], read_input [0xD4], status_bus [0xD7]) in order to simplify the Command_Line_Interface testing tool. This change does not affect either firmware or factory test development. I²C – Added that the write_protect command must always be accepted. I²C – OC and OT changed default value of hiccup to logic 1 Deleted POE compliant product availability Added improved input measurement capable product set.	Gabe Suranyi	Aug/15/2014
1.08	Deleted the footnote on temperature derating in the absolute ratings section. The note was incorrect and the derating should not be noted in two different sections. Added that at 277Vin the operational max ambient is 50°C	Gabe Suranyi	Aug/28/2014
1.09	I²C – added that vin_uv_fault_response is a read_only register I²C – Modified Status_word register to be consistent with the PMBus table, low_byte Vout,Iout, and Vin bits are Fault only. I²C – Fan control is changed to duty cycle only. I²C – Default Vin_uv_fault_limit changed to 80Vdc I²C – Added the black box feature	Gabe Suranyi	Sept/ 17/2014
1.10	I²C – Changed the default write_protect feature to allow all writes	Gabe Suranyi	Oct/02/2014
1.11	I²C – Changed mfr_revision from 7 to 6 bytes to avoid a conflict with the GE_interface_adapter firmware I²C – Changed the software_revision (0xE3) command to 7 bytes to be consistent with the GP protocol I²C – Further defined the black box data field space.	Gabe Suranyi	Oct/09/2014
1.12	Added a note that 5V standby should always be present and should be present before the main output is turned ON and should be terminated only after the main output has been turned OFF and PFW has been signaled. Tightened the regulation of the 5VDC output to ± 3% I²C – Added a note to read back; if insufficient time is allocated to return the requested data, the µC may return all FF's to thehost	Gabe Suranyi	Oct/15/2014

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1.13	I²C – Modified State Change Definition to: Any state change shall trigger an Alert asserted state. Deleted the following: Exceptions such as the OPERATION command. Reference to setting the Alert state of only the host in control. I²C – Fan default changed from 0x88 to 0x99.	Gabe Suranyi	Oct/27/2014
1.14	I²C – Under the functionality of Alert#, clearing the Alert when either the remote off/on or OPERATION off/on commands is executed has been removed. The Alert should get asserted whenever the unit state has changed. Additionally added that the rectifier will issue an Alert when its internal state has changed, even if that information cannot be reported by the status registers. (The status registers can only be cleared by the host controller. So a state change is not reported until first the registers are cleared by the host). I²C – Under State Change Definition, deleted the statements that if the power supply is back biased when input power returns an alert will not be generated and the statement regarding hot-plug operation because it is redundant. I²C – Added **AC Monitor Board communications fault** to the FAULT3 register I²C – Added that the factory default on startup is output ON [OPERATION ON] Clarified that the unit may be ON for a single fan fault as long as internal temperatures are within limits. The module_present signal is tied to logic_GRD. It does not have a 500Ω resistor in series. Aligned input current measurement accuracy limits with measurements taken during development.	Gabe Suranyi	Nov/12/2014
1.15	I²C – Deleted the restarted_ok bit of the STATUS2 register	Gabe Suranyi	Dec/01/2014
1.16	I²C – Changed low input voltage warning level and added note on hysteresis of the signal I²C –	Gabe Suranyi	Dec/05/2014
1.17	Changed input immunity to 25% line sag loading from FL to 75% load.	Gabe Suranyi	Jan/05/2015

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	V_{IN}	0	300	V_{AC}
Operating Ambient Temperature	T_A	-10	75	°C
Storage Temperature	T_{stg}	-40	85	°C
I/O Isolation voltage to Frame (100% factory Hi-Pot tested)			1500	V_{AC}

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, Vo=54V_{DC}, resistive load, and temperature conditions.

INPUT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Startup Voltage Low-line Operation High-line Operation	V_{IN}	80	85	90 185	V_{AC}
Operating Voltage Range Low-line Configuration High-line Configuration	V_{IN}	90 185	100 – 120 200 - 277	140 300	V_{AC}
Voltage Swell (no damage)	V_{IN}	305			V_{AC}
Turn OFF Voltage Hysteresis	V_{IN}	75 5	80	85	V_{AC}
Frequency	F_{IN}	47		66	Hz
Source Impedance (NEC allows 2.5% of source voltage drop inside a building)			0.2		Ω
Operating Current; at 110V_{AC} at 240V_{AC}	I_{IN}		15.5 16		A_{AC}
Inrush Transient (220V_{RMS}, 25°C, excluding X-Capacitor charging)	I_{IN}		25	40	A_{PK}
Idle Power (at 240V_{AC}, 25°C) 54V OFF 54V ON @ Io=0	P_{IN}		9 18		W
Leakage Current (300V_{AC}, 60Hz)	I_{IN}		2.5	3.5	mA
Power Factor (50 – 100% load)	PF	0.98	0.995		
Efficiency[1], 240V_{AC} @ 25°C 10% of FL 20% of FL 50% of FL FL	η	90 94 96 91			%
Holdup time (output allowed to decay down to 40V_{DC}) For loads below 1500W	T		10 15		ms
Ride through (at 240V_{AC}, 25°C)	T	1/2	1		cycle
Power Fail Warning[2] (main output allowed to decay to 40V_{DC})	PFW	3	5		ms
Isolation (per EN60950) (consult factory for testing to this requirement) Input-Chassis/Signals Input - Output	V	1500 3000			V_{AC} V_{AC}

[1] Fan disabled, 5V output at 0 load.

[2] Internal protection circuits may override the PFW signal and may trigger an immediate shutdown.

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Electrical Specifications (continued)

$54V_{DC}$ MAIN OUTPUT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Power @ low line input 100 – $120V_{AC}$ @ high line input 200 – $277V_{AC}$	W	1500 3000/3500			W_{DC}
Factory set default set point	V_{OUT}		54		V_{DC}
Overall regulation (load, temperature, aging) 0 - 45°C LOAD > 2.5A > 45°C	V_{OUT}	-1 -2		+1 +2	%
Output Voltage Set Range[3] - analog margining - Set either by I^2C or RS485	V_{OUT}	44 42		58 58	V_{DC}
Output Current - @ 1500W (100 – 120Vac), 54V/52V @ 3000W (200 – $277V_{AC}$), 54V/52V @ 3500W (200 – $277V_{AC}$), 54V/52V	I_{out}	1 1 1		27.8/28.9 55.5/57.8 64.8/67.3	A_{DC}
Current Share (> 50% FL)		-5		5	%FL
Proportional Current Share between different rectifiers[4] (> 50% FL)			<7		%FL
Output Ripple (20MHz bandwidth, load > 1A) RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz) Psophometric Noise	V_{OUT}			 100 250[5] 9[6]	 mV_{rms} mV_{p-p} mV_{rms}
External Bulk Load Capacitance	C_{OUT}	0		5,000	µF
Turn-On (monotonic turn-ON from 30 – 100% of Vnom above 5°C) Delay Rise Time – PMBus mode Rise Time - RS-485 mode[7] Output Overshoot	 T V_{OUT}		 5 100 5		 s ms s %
Load Step Response ($I_{O,START}$ > 2.5A) ΔI[8] ΔV, V_{AC} < 285_{AC} ΔV, V_{AC} ≥ 285_{AC} Response Time	 I_{OUT} V_{OUT} V_{OUT} T		 2.0 3.2 2	 50	 %FL V_{DC} V_{DC} ms
Overload - Power limit @ high line down to $52V_{DC}$ Power limit @ low line down to $52V_{DC}$ High line current limit[9] if V_{out} > $39V_{DC}$ [3000W/3500W] Low line current limit Output shutdown (commences as voltage decays below this level)	P_{OUT} P_{OUT} I_{OUT} I_{OUT} V_{OUT}	3000/3500 1500 59/68 30		 36	W_{DC} W_{DC} A_{DC} A_{DC} V_{DC}
System power up	Upon insertion the rectifier will delay an overload shutdown for 20 seconds allowing for the insertion and startup of multiple rectifiers within a system.				
Overvoltage - 200ms delayed shutdown Immediate shutdown	V_{OUT}	> 65		< 60	V_{DC}
Latched shutdown	Three restart attempts are implemented within a 1 minute window prior to a latched shutdown.				
Over-temperature warning (prior to commencement of shutdown) Shutdown (below the max device rating being protected) Restart attempt Hysteresis (below shutdown level)	T		5 20 10		°C
Isolation Output-Chassis (Standard, non-POE compliant) Output-Chassis/Signals (POE compliant per IEEE802.3)	V	500 2250			V_{DC} V_{DC}

[3] When V_O > 57V power derating starts at 50°C

[4] With existing CP platform of rectifiers

[5] 500mVp-p max above $280V_{AC}$, $300mV_{p-p}$ max for POE product

[5] Complies with ANSI TI.523-2001 section 4.9.2 emissions max limit of 20mV flat unweighted wideband noise limits

[7] Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.

[8] di/dt (output current slew rate) 1A/µs.

[9] Above $280V_{AC}$ the current limit reduces to 50A when V_{OUT} ≤ $45V_{DC}$ and to 25A when V_{OUT} ≤ $45V_{DC}$ and T_{AMB} > 55C.

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$5V_{DC}$ Auxiliary output					
Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint	V_{OUT}		5		V_{DC}
Overall Regulation		-3		+3	%
Output Current		0.005		2	A
Ripple and Noise (20mHz bandwidth)			50	100	mV_{p-p}
Over-voltage Clamp				7	V_{DC}
Over-current Limit		110		175	%FL

The $5V_{DC}$ should be ON before availability of the $54V_{DC}$ main output and should turn OFF only if insufficient input voltage exists to provide reliable $5V_{DC}$ power. The PFW signal should have indicated a warning that power would get turned OFF and the $54V_{DC}$ main output should be OFF way before interruption of the $5V_{DC}$ output.

General Specifications

Parameter	Min	Typ	Max	Units	Notes
Reliability		450,000		Hours	Full load, 25°C ; MTBF per SR232 Reliability protection for electronic equipment, issue 2, method I, case III,
Service Life		10		Years	Full load, excluding fans
Unpacked Weight		2.18/4.8		Kgs/Lbs	
Packed Weight		2.45/5.4		Kgs/Lbs	
Heat Dissipation	190 Watts or 648 BTUs @ 80% load, 250 Watts or 853 BTUs @ 100% load				

Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. Signals are referenced to Logic_GRD unless noted otherwise. Fault, PFW, OTW, and Alert need to be pulled HI through external pull-up resistors.

Parameter	Symbol	Min	Typ	Max	Unit
ON/OFF 54V output OFF	V_{OUT}	1.4	—	5	V_{DC}
54V output ON (should be connected to Logic_GRD)	V_{OUT}	0	—	0.5	V_{DC}
Margining (through adjusting Vprog)		44		58	V_{DC}
Voltage control range	$V_{control}$	0		3.3	V_{DC}
Programmed output voltage range	V_{OUT}	44		58	V_{DC}
Voltage adjustment resolution (8-bit A/D)	$V_{control}$		3.3		mV_{DC}
Output configured to $54V_{DC}$	$V_{control}$	3.0		3. 3	V_{DC}
Output configured to $44V_{DC}$	$V_{control}$	0		0.1	V_{DC}
Interlock [short pin shorted to VOUT(-) on system side]					
54V output OFF	$V_{control}$	1.4	—	5	V_{DC}
54V output ON	$V_{control}$	0	—	0.8	V_{DC}
Module Present [short pin to Logic_GRD internally]					
Over Temperature Warning (OTW#) Logic HI (temperature normal)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current	I	—	—	5	mA
Logic LO (temperature is too high)	V	0	—	0.4	V_{DC}
Fault# Logic HI (No fault is present)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current	I	—	—	5	mA
Logic LO (Fault is present)	V	0	—	0.4	V_{DC}
Alert# (Alert#_0, Alert#_1) Logic HI (No Alert - normal)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current	I	—	—	5	mA
Logic LO (Alert# is set)	V	0	—	0.4	V_{DC}

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Feature Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Protocol select Logic HI - Analog/PMBus™ mode Logic – intermediate – RS485 mode Logic LO – DSP reprogram mode	V_{IH} V_{II} V_{IL}	2.7 1.0 0	— —	3.5 2.65 0.4	V_{DC} V_{DC} V_{DC}

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics[10]						
Input Logic High Voltage (CLK, DATA)		V	1.5		3.6	V_{DC}
Input Logic Low Voltage (CLK, DATA)		V	0		0.8	V_{DC}
Input high sourced current (CLK, DATA)		I	0		10	µA
Output Low sink Voltage (CLK, DATA, ALERT#)	I_{OUT}=3.5mA	V			0.4	V_{DC}
Output Low sink current (CLK, DATA, ALERT#)		I	3.5			mA
Output High open drain leakage current (CLK,DATA, ALERT#)	V_{OUT}=3.6V	I	0		10	µA
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz
Measurement System Characteristics						
Clock stretching		$T_{stretch}$			25	ms
I_{OUT} measurement range		I_{rng}	0		80	A_{DC}
I_{OUT} measurement accuracy 25°C	> 12.8A < 12.8A	$I_{out(acc)}$	-1 5		+1 5	% of FL %
I_{OUT} measurement accuracy 0 - 40°C[11]	> 12.8A	$I_{out(acc)}$	-2		+2	% of FL
V_{OUT} measurement range		$V_{out(rng)}$	0		70	V_{DC}
V_{OUT} measurement accuracy[12]		$V_{out(acc)}$	-1		+1	%
Temp measurement range		$Temp_{(rng)}$	0		150	°C
Temp measurement accuracy[13]		$Temp_{(acc)}$	-4		+4	°C
V_{IN} measurement range		$V_{in(rng)}$	0		320	V_{AC}
V_{IN} measurement accuracy @ 25°C		$V_{in(acc)}$	-1.25		+1.25	%
I_{IN} measurement range		$I_{in(rng)}$	0		30	I_{AC}
I_{IN} measurement accuracy - standard measurement @ 25°C		$I_{in(acc)}$	-3		+3	% of FL
I_{IN} measurement accuracy - improved measurement @ 25°C	> 300W 100 – 300W < 300W	$I_{in(acc)}$	-1.25 -2.5 -5	 1.5 2.5	+1.25 +2.5 +5	%
P_{IN} measurement range		$P_{in(rng)}$	0		4000	W_{in}
P_{IN} measurement accuracy – standard measurement @ 25°C	> 300W < 300W	$P_{in(acc)}$	-5	 15	+5 30	% W
P_{IN} measurement accuracy – improved measurement @ 25°C	> 300W 100 – 300W < 100W	$P_{in(acc)}$	-1.25 -2.5 -10	1 1.5 3	+1.25 +2.5 10	% % W
Fan Speed measurement range			0		30k	RPM
Fan Speed measurement accuracy			-10		10	%
Fan speed control range			0		100	%

[10] Clock, Data, and Alert# need to be pulled up to V_{DD} externally.

[11] **Below 20% of FL;** 10 – 20% of FL: ±0.64A; 5 – 10% of FL: ±0.45A; 2.5 – 5% of FL: ±0.32A.

[12] Above 2.5A of load current

[13] Within 30° of the default warning and fault levels.

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Environmental Specifications

Parameter	Min	Typ	Max	Units	Notes
Ambient Temperature	-40[14]		55[15]	°C	Air inlet from sea level to 5,000 feet.
Exhaust Air Temperature			15	°C	Maximum allowed internal temperature rise
Storage Temperature	-40		85	°C	
Operating Altitude			1524/5000	m / ft	
Non-operating Altitude			8200/30k	m / ft	
Power Derating with Temperature			2.0	%/°C	55°C to 75°C
Power Derating with Altitude			2.0	°C/305 m °C/1000 ft	Above 1524/5000 m/ft; 3962/13000 m/ft max
Acoustic noise		55		dbA	Full load
Over Temperature Protection		125/110		°C	Shutdown / restart [internally measured points]
Humidity Operating Storage	 5 5		 95 95	 % %	Relative humidity, non-condensing
Shock and Vibration acceleration			2.4	Grms	IPC-9592B, Class II

EMC

Parameter	Criteria	Standard	Level	Test
AC input[16]	Conducted emissions	EN55022, FCC Docket 20780 part 15, subpart J EN61000-3-2 Meets Telcordia GR1089-CORE by a 3dB margin	A +6dB	0.15 – 30MHz 0 – 2 KHz
	Radiated emissions	EN55022	A +6dB	30 – 10000MHz
Parameter	**Criteria**	**Standard**	**Criteria[17]**	**Test**
AC Input Immunity	Line sags and interruptions	EN61000-4-11	B	-30%, 10ms
			B	-60%, 100ms
			B	-100%, 5sec
		Output will stay above 40V_{DC} @ 75% load Sag must be higher than 80Vrms.	A	25% line sag for 2 seconds 1 cycle interruption
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free	A	4kV, common mode
			A	2kV, differential mode
		ANSI C62.41 - level A3	B	6kV, common & differential
	Fast transients	EN61000-4-4, Level 3	B	5/50ns, 2kV (common mode)
Enclosure immunity	Conducted RF fields	EN61000-4-6, Level 3	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3, Level 3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140	A	
	ESD	EN61000-4-2, Level 4	B	8kV contact, 15kV air

[14] Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -5°C

[15] At 277V input line operation the maximum ambient is reduced to 50°C. See operational limitations in other sections of this document

[16] Emissions requirements can be verified using either the J2007001 or J85480 GE shelf. Standalone the additional margin is not required.

[17] Criteria A: Normal performance Within limits. Criteria B: Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention.

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Input: 100-120/220-277 Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

Characteristic Curves

The following figures provide typical characteristics for the CP3500AC54TE rectifier and 25ºC.

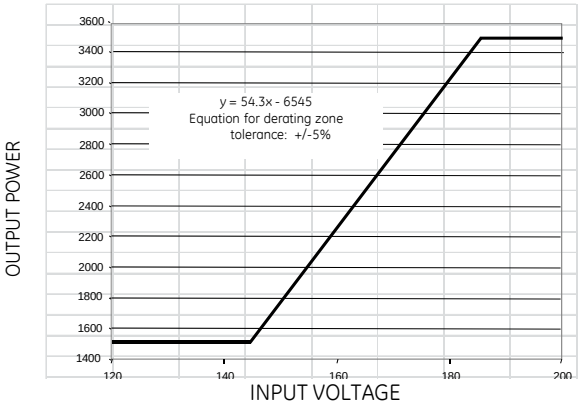

Figure 4. 54V_{DC} output: Output power derating based on input voltage.

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Control and Status

The Rectifier provides three means for monitor/control: analog, PMBus™, or the GE Galaxy-based RS485 protocol.

Details of analog control and the PMBus™ based protocol are provided in this data sheet. GE will provide separate application notes on the Galaxy RS485 based protocol for users to interface to the rectifier. Contact your local GE representative for details.

Control hierarchy: Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (Vprog) and a PMBus command, (OPERATION) .

Unless otherwise noted, the signal pin controls the feature until the firmware command is executed. However, once the firmware command has been executed, the signal pin is ignored. In the above example, the rectifier will no longer 'listen' to the Vprog pin if the OPERATION command has been executed.

In summary, Vprog is utilized for initialized configuration of the output voltage and to change the output voltage when PMBus is not used for that function.

Signal Reference: Unless otherwise noted, all signals are referenced to Logic_GRD. See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic_GRD is isolated from the main output of the rectifier for PMBus communications. Communications and the 5V standby output are not connected to main power return (Vout(-)) and can be tied to the system digital ground point selected by the user. (Note that RS485 communications is referenced to Vout(-), main power return of the rectifier).

Logic_GRD is capacitively coupled to Frame_GRD inside the rectifier. The maximum voltage differential between Logic_GRD and Frame_GRD should be less than $100V_{DC}$.

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $10V_{DC}$ the Output LED will continue blinking.
When output voltage is < $10V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Auto restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Restart after a latchoff: **PMBus™** fault_response commands can be configured to direct the rectifier to remain latched off for over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON**.**
2. The unit may be commanded to restart via i2c through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart.**

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Control Signals

Protocol: This signal pin defines the communications mode setting of the rectifier. Three different states can be configured. State #1 is the I²C application in which case the protocol pin should be left a no-connect. State #2 is the RS485 mode application in which case a resistor value between 1kΩ and 5kΩ should be present between this pin and Vout (-). State #3 is the re-program state in which case a short should be applied between this pin and Vout (-).

Device address in I²C mode: Address bits A3, A2, A1, A0 set the specific address of the µP in the rectifier. With these four bits, up to sixteen (16) rectifiers can be independently addressed on a single I²C bus. These four bits are configured by two signal pins, Unit_ID and Rack_ID. The least significant bit x (LSB) of the address byte is set to either **write [0]** or ***read [1]***. A ***write*** command instructs the rectifier. A ***read*** command accesses information from the rectifier.

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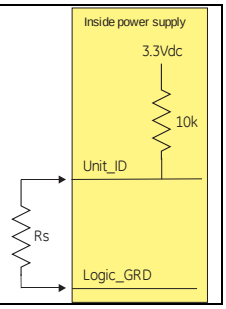
CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
uP	40 – 4F	1	0	0	A3	A2	A1	A0	R/W
Broadcast	00	0	0	0	0	0	0	0	0
ARA[18]	C	0	0	0	1	1	0	0	1
		MSB							LSB

Unit_ID: Up to 10 different units are selectable.

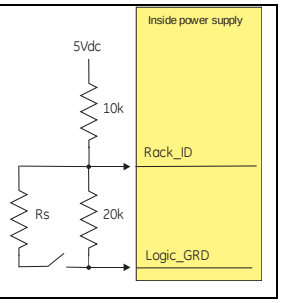
A voltage divider between 3.3V and Logic_GRD configures Unit_ID. Internally a 10kΩ resistor is pulled up to 3.3VDC. A pull down resistor Rs needs to be connected between pin Unit_ID and Logic_GRD.



Unit_ID	Voltage level	R_S (± 0.1%)
Invalid	3.30	
1	3.00	100k
2	2.67	45.3k
3	2.34	24.9k
4	2.01	15.4k
5	1.68	10.5k
6	1.35	7.15k
7	1.02	4.99k
8	0.69	2.49k
9	0.36	1.27k
10	0	0

Rack_ID: Up to 8 different combinations are selectable.

A voltage divider between $5V_{DC}$ and Logic_GRD configures Rack_ID. The 10k-20kΩ divider sets the initial voltage level to $3.3V_{DC}$. A switch between each R_S value changes the Rack_ID level according to the table below.



Rack_ID	Voltage level	R_S (± 0.1%)
1	3.3	open
2	2.8	35.2k
3	2.3	15k
4	1.8	8k
5	1.4	4.99k
6	1	2.87k
7	0.5	1.27k
8	0	0

Configuration of the A3 – A0 bits: The rectifier will determine the configured address based on the Unit_ID and Rack_ID voltage levels as follows (the order is A3 – A0):

		Unit_ID				
		1	2	3	4	5
Rack_ID	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
	4	1100	1101	1110	1111	
	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

Unit x Shelf: 4 x 4 and 5 x 3

		Unit_ID				
		6	7	8	9	10
Rack_ID	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
	4	0110	0111	0000	0001	0010
	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

Unit x Shelf: 2 x 8 and 3 x 5

Address detection: The **Slot_ID** pin must be shorted to **Vout(-)** in order to deliver output power. This connection provides a second interlock feature. (In RS485 mode the **slot_ID** resistance to **Vout(-)** is sufficient to sense the interlock feature)

[18] Implement if feasible, this is a 'read' only address

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Device address in RS485 mode: The address in RS485 mode is divided into two components; Unit_ID as described above under i²c addressing, Slot_ID and Shelf_ID

Bay_ID: The Unit_ID definition in I²C mode becomes the bay id in RS485 mode.

Slot_ID: Up to 10 different rectifiers could be positioned across a 19" shelf if the rectifiers are located vertically within the shelf. The resistor below needs to be placed between Slot_ID and Vout (-). Internal pull-up to 3.3V is 10kΩ.

Slot	Resistor	Voltage
invalid	none	3.3V
1	100k	3V
2	45.3k	2.67V
3	24.9k	2.34V
4	15.4k	2.01V
5	10.5k	1.68V

Slot	Resistor	Voltage
6	7.15k	1.35V
7	4.99k	1.02V
8	2.49k	0.69V
9	1.27k	0.36V
10	0	0

Shelf_ID: When placed horizontally up to 10 shelves can be stacked on top of each other in a fully configured rack. The shelf will generate the precision voltage level tabulated below referenced to Vout (-).

Shelf	V_{MIN}	V_{NOM}	V_{MAX}
1	2.3	2.5	2.7
2	4.7	5.0	5.3
3	7.4	7.5	7.6
4	9.5	10.0	10.5
5	11.8	12.5	13.2
6	14.2	15.0	15.8
7	16.6	17.5	18.4
8	19	20.0	21
9	21.3	22.5	23.6
10	23.8	25.0	26.3

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A ***read*** instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth *acknowledge* bit. To be certain that each rectifier responded to the global instruction, a *READ* instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Alert Response Address (ARA): This feature enables the 'master' to rapidly determine which 'slave' rectifier triggered the Alert# signal without having to poll each rectifier one at a time. During normal operation the rectifier activates (pulls down LO) the Alert# signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the alert-response-address, address 12b, with a 'read' instruction. If the rectifier triggered the 'alert' it should respond back with its address. The instruction takes the form below;

1	8		1	8	1	8	1	1
S	ARA address	Rd	A	My address	A	PEC	A	P

If during the ARA response multiple rectifiers send out their addresses, then the actual address received by the master is the lowest address from the combinations of those rectifiers that responded.

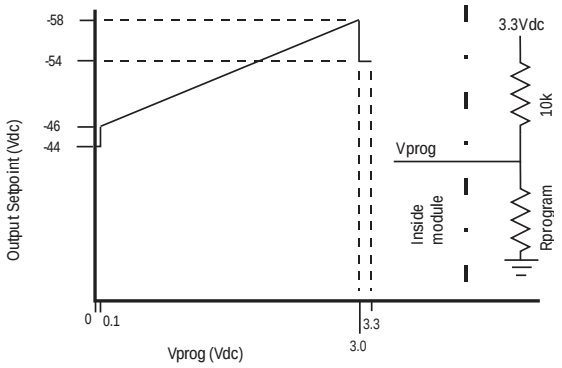
The 'my address' field contains the address of the rectifier in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification

The µC needs to read the actual **my address** data byte that is sent back to the master. If the **my address** data byte agrees with the address of this unit, then, and only then, the µC needs to clear (de-assert) its Alert# signal. Thus, the rectifier whose address has been sent out gets de-asserted from the joint Alert# line.

If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all rectifiers that asserted Alert# have had their status states read back.

Voltage programming (V_{prog}): Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Software voltage programming permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

An analog voltage on this signal can vary the output voltage from 44Vdc to 58Vdc.



Factory default setting driven by Vprog

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The Vprog pin level should be set by a divider from 3.3Vdc to Logic_GRD external to the rectifier as shown in the graph. Programming can be accomplished either by a resistor divider or by a voltage source injecting a precision voltage level into the Vprog pin. Above 3Vdc the rectifier sets the output to its default state.

Hardware voltage programming controls the output voltage until a software margin command is executed. Software voltage programming (margining) permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

When bias power is recycled to the controller the controller restarts into its default configuration, programmed to set the output as instructed by the V_{prog} pin. Again, subsequent software commanded settings permanently override the margin setting. As an example, adding a resistor between V_{prog} and Logic_GRD is an effective way of changing the factory set point of the rectifier to whatever voltage level is desired by the user during initial start-up.

Load share (Ishare): This is a single wire analog signal that is generated and acted upon automatically by rectifiers connected in parallel. Ishare pins should be connected to each other for rectifiers, if active current share among the rectifiers is desired. No resistors or capacitors should get connected to this pin.

ON/OFF: Controls the main $54V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn **ON** the rectifier. The rectifier will turn **OFF** if either the **ON/OFF** or the **Interlock** pin is released. This signal is referenced to Logic_GRD. Note that in RS485 mode this pin is ignored.

Interlock: This is a shorter pin utilized for hot-plug applications to ensure that the rectifier turns **OFF** before the power pins are disengaged. It also ensures that the rectifier turns **ON** only after the power pins have been engaged. Must be connected to V_OUT (-) for the rectifier to be ON.

Module Present: This signal is tied to Logic_GRD inside the rectifier. It's intent is to provide a signal to the system that a rectifier is physically present in the slot.

8V_INT: Single wire connection between rectifiers, Provides bias to the DSP of an unpowered rectifier.

Protocol: Establishes the communications mode of the rectifier, between analog/PMBus and RS485 modes. For RS485, connect a 10kΩ pull-down resistor from this pin to V_OUT(-). For analog/PMBus leave the pin open. Do not tie this signal pin to V_OUT(-) because that connection configures the internal DSP into a reprogrammed state.

Status Signals

Power Fail Warning (PFW#): This signal is HI when the main output is being delivered and goes LO for the duration listed in this data sheet prior to the output decaying below the listed voltage level. PFW also pulses at a 1ms duty cycle if the unit is in overload.

Fault#: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Fan failure
- Over-temperature warning
- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

Over temp warning (OTW#): A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the rectifier. In its default configuration, the unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

Alert#: A TTL compatible status signal, This signal needs to be pulled HI externally through a resistor.

Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'Logic_GRD'.

Pull-up resistors: The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I²C and SMBus standards.

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

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Digital Feature Descriptions

PMBus™ compliance: The rectifier is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from www.pmbus.org.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

The Alert# response protocol (ARA) whereby the PMBus Master can inquire who activated the Alert# signal is also supported. This feature is described in more detail later on.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller.

If a non-supported read is requested the rectifier will return 0x00h for data.

Data out-of-range: The rectifier validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the MASTER. Rectifiers are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' µController inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.

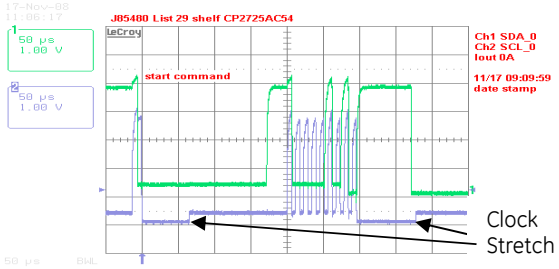

Figure 15. Example waveforms showing clock stretching.

I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The rectifiers default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

Alert#: The rectifier can issue Alert# driven from either its internal micro controller (µC) or from the I²C bus master selector stage. That is, the Alert# signal of the internal µC funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the rectifier. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The µC driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear_faults' instruction.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults

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Alert#_0 , the defaulted I²C side in control, is asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled.

The rectifier will re-assert the Alert line if the internal state of the power supply has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the power supply. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Re-initialization: The I²C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I²C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I²C µController may not recognize a command sent to it. (i.e. a start condition).

Read back delay: The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A ***read*** instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth *acknowledge* bit. To be certain that each rectifier responded to the global instruction, a *READ* instruction should be executed to each rectifier to verify that the command properly executed.

The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Alert Response Address (ARA): This feature enables the 'master' to rapidly determine which 'slave' rectifier triggered the Alert# signal without having to poll each rectifier one at a time. During normal operation the rectifier activates (pulls down LO) the Alert# signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the alert-response-address, address 12b, with a 'read' instruction. If the rectifier triggered the 'alert' it should respond back with its address. The instruction takes the form below;

1	8		1	8	1	8	1	1
S	ARA address	Rd	A	My address	A	PEC	A	P

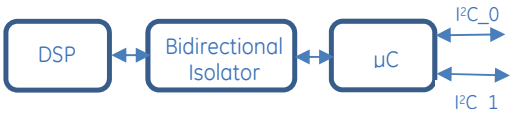
If during the ARA response multiple rectifiers send out their addresses, then the actual address received by the master is the lowest address from the combinations of those rectifiers that responded.

The 'my address' field contains the address of the rectifier in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification

The µC does not have the ability to listen to the actual address that is sent over the bus, if multiple 'slaves' respond simultaneously, and therefore it does not clear its Alert# line. The host should read the status of the rectifier whose address was actually sent across the bus. Reading either the read_status [0 x D0] or status_word [0 x 79] would clear the Alert# line of the rectifier that was addressed. The rectifier will not re-assert the Alert# line unless the status states actually changed.
If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all rectifiers that asserted Alert# have had their status states read back.

Dual, redundant buses: Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time.

Conceptually a Digital Signal Processor (DSP) referenced to Vout(-) of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power GRD, Vout(-) and signal GRD (Logic_GRD). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I2C lines to two independent system controllers.



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The secondary micro controller is designed to default to I2C_0 when powered up. If only a single system controller is utilized, it should be connected to I2C_0. In this case the I2C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I2C_0 and the other to I2C_1.

At power up the master connected to I2C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

☐ Master to Slave ☐ Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	NA	P

Block communications: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	A	P

Block read format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	NA	P

Linear Data Format: The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^E$$

Where: V is the value, M is the 11-bit, two's complement mantissa, *E* is the 5-bit, two's complement exponent

Standard features

Supported features that are not readable: The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both the CNTL pin, and the OPERATION command, enabling or disabling the output, are supported. Other options are not supported.
Capability (0x19)	400KHz, ALERT#
PMBus revision (0x98)	1.2

Status and Alarm registers: The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

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CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

PMBus™ Command set:

Command	Hex Code	Data Field	Non-Volatile Memory Storage[19] / Default
Operation	0x01	1	Yes/80
Clear_Faults	0x03	0	
Write _Protect	0x10	1	Yes/00
Restore_default_all	0x12	0	
Restore_user_all	0x16	x	
Store_user_code	0x17	1	yes
Restore_user_code	0x18	1	
Vout_mode	0x20	1	
Vout_command	0x21	2	yes
Vin_ON	0x35	2	
Vin_OFF	0x36	2	
Fan_config_1_2	0x3A	1	Yes /99
Fan_command_1	0x3B	2	
Vout_OV_fault_limit	0x40	2	Yes / 60
Vout_OV_fault_response	0x41	1	No / 80
Vout_OV_warn_limit	0x42	2	Yes / 59
Vout_UV_warn_limit	0x43	2	Yes / 42
Vout_UV_fault_limit	0x44	2	Yes /41
Vout_UV_fault_response	0x45	1	No / C0
Iout_OC_fault_limit	0x46	2	Yes / 68
Iout_OC_fault_response[20]	0x47	1	Yes / F8
Iout_OC_LV_fault_limit	0x48	2	Yes/36
Iout_OC_warn_limit	0x4A	2	Yes / 67.3
OT_fault_limit	0x4F	2	Yes/TBD
OT_fault_response[21]	0x50	1	Yes / C0
OT_warn_limit	0x51	2	Yes/TBD
Vin_OV_fault_limit	0x55	2	No/ 300
Vin_OV_fault_response	0x56	1	No/ C0
Vin_OV_warn_limit	0x57	2	Yes / 295
Vin_UV_warn_limit[22]	0x58	2	Yes / 87.5
Vin_UV_fault_limit[23]	0x59	2	No / 80
Vin_UV_fault_response	0x5A	1	No/ C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_Vout	0x7A	1	
Status_Iout	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Status_fans_1_2	0x81	1	
Read_Vin	0x88	2	
Read_Iin	0x89	2	

Command	Hex Code	Data Field	Non-Volatile Memory Storage/ Default
Read_Vout	0x8B	2	
Read_Iout	0x8C	2	
Read_temp_PFC	0x8D	2	
Read_temp_dc_pri	0x8E	2	
Read_temp_dc_sec	0x8F	2	
Read_fan_speed_1	0x90	2	
Read_fan_speed_2	0x91	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	5	
Mfr_model	0x9A	15	
Mfr_revision	0x9B	6	
Mfr_serial	0x9E	15	
Status_summary	0xD0	13	
Status_unit	0xD1	2	
Status_alarm	0xD2	3	
Read_fan_speed	0XD3	4	
Read_input	0xD4	4	
Read_firmware_rev	0xD5	6	
Read_run_timer	0xD6	3	
Status_bus	0xD7	1	
Take_over_bus_control	0xD8		yes
EEPROM Record	0xD9	128	yes
Read_temp_exhaust	0xDA	2	
Read_ temp_inlet	0xDB	2	
Reserved for factory use	0XDC		
Reserved for factory use	0XDD		
Reserved for factory use	0XDE		
Test_Function	0xDF	1	
Upgrade commands			
Password	0xE0	4	
Target_list	0xE1	4	
Compatibility_code	0xE2	16	
Software_version	0xE3	7	
Memory_capability	0xE4	7	
Application_status	0xE5	1	
Boot_loader	0xE6	1	
Data_transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

[19] Yes – indicates that the data can be changed by the user

[20] Only latched (0xC0) or hiccup (0xF8) are supported

[21] Only latched (0x80) or restart (0xC0) are supported

[22] Recovery set at 90V

[23] Recovery set at 86V

Command Descriptions

Operation (0x01) : Turns the 54V output ON or OFF. The default state is **ON** at power up. Only the following data bytes are supported:

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

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To **RESET** the rectifier using this command, command the rectifier OFF, wait at least 2 seconds, and then command the rectifier back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (0x03): Clears all STATUS and FAULT registers and resets the Alert# line of the I^2C side in control. The I^2C side not in control cannot clear registers in the power supply. This command is always executable.

If a fault still persists after the issuance of the clear_faults command, the specific registers indicating the fault are reset and, the Alert# line is activated again.

WRITE_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code command. The default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

Restore_Default_All (0x12): Restores all operating register values and responses to the factory default parameters set in the rectifier. The factory default cannot be changed.

Restore_default_code (0x14): Restore only a specific register parameter into the operating register section of the rectifier.

Store_user_code (0x17): Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

Restore_user_code (0x18): Restores the user default setting of a single register.

Vout_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bit mantissa. The exponent is fixed by the rectifier and is returned by this command

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	xxxxxb

Vout_Command (0x21) : Used to dynamically change the output voltage of the rectifier. This command can also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all rectifiers using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the **Vprog** signal pin. The program no longer looks at the '**Vprog** pin' and will not respond to any hardware voltage settings. If power is removed from the µController it will reset itself into its default configuration looking at the **Vprog** signal for output voltage control. In many applications, the **Vprog** pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once I^2C communications are established.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the Vprog pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Programmed voltage range: $42V_{DC}$ – $58\ V_{DC}$.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

The constants for voltage programming are: m = 400, b and R = 0. Multiply the desired set point by the m constant, 50.45 x 400 = 20,180. Convert this binary number to its hex equivalent: 20,180b = 4ED4h. Transmit the data LSB first, followed by MSB, 0 x D44Eh.

Vin_ON (0x35): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Vin_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Fan_config_1_2 (0x3A) : This command requires that the fan speed be commanded by duty cycle. Both fans must be commanded simultaneously. The tachometer pulses per revolution is not used. Default is duty cycle control.

Fan_command_1 (0x3B): This command instructs the rectifier to increase the speed of both fans above what is internally required. The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e. 100% = 0 x 64h. The

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command can increase or decrease fan speed. An incorrect value will result in a 'data error'.

Sending 00h tells the rectifier to revert back to its internal control.

Fan_command_2 (0x3C): not used in this rectifier. Issuing this command will result in 'invalid command'.

Vout_OV_fault_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV_fault value is set at 60Vdc. This level can be permanently changed and stored in non-volatile memory.

Vout_OV_fault_response (0x41): This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

Restart after a latched state: Either of four restart mechanisms is available;

- The hardware pin **ON/OFF** may be cycled OFF and then ON.
- The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON .
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the **ON/OFF** signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Vout_OV_warn_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at 56Vdc. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_warn_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at 41Vdc. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level. The default UV_fault limit is set at 36Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_response (0x45): Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Iout_OC_fault_limit (0x46): Sets the value at which the rectifier will shut down at High Line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 30A.

Iout_OC_fault_response (0x47): Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state can be permanently changed and stored in non-volatile memory. The response is the same for both low_line and high_line operations.

Iout_OC_warn_limit (0x4A): Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level at high line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 29A.

OT_fault_limit (0x4F): Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT_fault_response register.

OT_fault_response (0x50): Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51): Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

Vin_OV_fault_limit (0x55): Sets the value at which the rectifier shuts down because the input voltage exceeds the allowable operational limit. The default Vin_OV_fault_limit is set at

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300Vac. This level can be permanently lowered and stored in non-volatile memory.

Vin_OV_fault_response (0x56): Sets the response if the input voltage level exceeds the Vin_OV_fault_limit value. The default Vin_OV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Vin_UV_warn_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is 90Vac. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

Vin_UV_fault_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin_UV_fault_limit is set at 85Vac. This level can be permanently raised and stored in non-volatile memory

Vin_UV_fault_response (0x5A): Sets the response if the input voltage level falls below the Vin_UV_fault_limit value. The default Vin_UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

STATUS_BYTE (0x78) : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Unit is busy	0
6	OUTPUT OFF	0
5	VOUT Overvoltage Fault	0
4	IOUT Overcurrent Fault	0
3	VIN Undervoltage Fault	0
2	Temperature Fault or Warning	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

STATUS_WORD (0x79): Returns status_byte as the low byte and the following high_byte.

Bit Position	Flag	Default Value
7	VOUT Fault or Warning	0
6	IOUT Fault or Warning	0
5	INPUT Fault or Warning	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	FAN Fault or Warning	0
1	OTHER	0
0	UNKNOWN Fault or Warning	0

STATUS_VOUT (0X7A): Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	VOUT_OV_WARNING	0
5	VOUT_UV_WARNING	0
4	VOUT UV Fault	0
3 - 0	X	0

STATUS_IOUT (0X7B): Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	IOUT OC LV Fault	0
5	IOUT OC Warning	0
4	X	0
3	CURRENT SHARE Fault	0
2	IN POWER LIMITING MODE	0
1 - 0	X	0

The OC Fault limit sets where current limit is set. The rectifier actually shuts down below the LV fault limit setting.

STATUS_INPUT (0X7C): Returns one byte of information of input voltage related faults.

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_ Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1 - 0	X	0

STATUS_TEMPERATURE (0x7D): Returns one byte of information of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 - 0	X	0

STATUS_CML (0X7E): Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 - 2	X	0
1	Other Communication Fault	0
0	X	0

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STATUS_fans_1_2 (0X81): Returns one byte of information of fan status.

Bit Position	Flag	Default Value
7	Fan 1 fault	0
6	Fan 2 fault	0
5 - 4	X	0
3 - 2	Fan 1 & 2 speed overwritten	0
1 - 0	X	0

Read back Descriptions

Single parameter read back: Functions can be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1
Sr	Slave address	Rd	A

8	1	8	1	8	1	1
LSB	A	MSB	A	PEC	No-Ack	P

Read back error: If the µC does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read_fan_speed 1 & 2 (0x90, 0x91): Reading the fan speed is in Direct Mode returning the RPM value of the fan.

Read_FRU_ID (0x99,0x9A,0x9B,0x9E): Returns FRU information. Must be executed one register at a time.

1	8		1	8	1
S	Slave address	Wr	A	Command 0x9x	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = x	A

8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	No-Ack	P

Mfr_ID (0x99): Manufacturer in ASCII – 5 characters maximum, General Electric – Critical Power represented as, GE-CP

Mfr_ID (0x9A): Manufacturer model-number in ASCII – 16 characters, for this unit: CP3500AC54TExxxx

Mfr_revision (0x9B): Total 7 bytes, provides the product series number when the product was manufactured.

Mfr_serial (0x9E): Product serial number includes the manufacturing date, manufacturing location in up to 15 characters. For example:

13KZ51018193xxx, is decoded as;

13 – year of manufacture, 2013

KZ – manufacturing location, in this case Matamoros

51 – week of manufacture

018193xxx – serial #, mfr choice

Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Mfr_Specific Status and alarm registers: The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

Status_summary (0xD0) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 11	A

8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1
Current-LSB	A	Current-MSB	A

8	1	8	1
Temperature-LSB	A	Temperature-MSB	A

8	1	1
PEC	No-Ack	P

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CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277 Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

Status_unit(0xD1): This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

Status-2

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	Power_Capacity [HL = 1]	x
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	x

Oring fault: Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the power supply. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus a non-destructive or'ing fault does not trigger a shutdown.

Status-1

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	Service LED ON	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	x

Status_alarm (0xD2): This command returns the ALARM-3 - ALARM-1 register values.

Alarm-3

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i2c communications fault	0
3	AC monitor communications fault	0
2	x	0
1	x	0
0	Or'ing fault	0

Alarm-2

Bit Position	Flag	Default Value
7	FAN_Fault	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	Vo lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

Power Delivery: If the internal sourced current to the current share current is > 10A, a fault is issued.

Alarm-1

Bit Position	Flag	Default Value
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

Read_Fan_speed (0 x D3) : Returns the commanded speed in percent and the measured speed in RPM. If a fan does not exist, or if the command is not supported the unit return 0x00.

1	8		1	8	1
S	Slave address	Wr	A	Command 0xE1	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 6	A

8	1	8	1	8	1	8	1
Adj%-LSB	A	Adj%-MSB	A	Fan1-LSB	A	Fan1-MSB	A

8	1	8	1	8	1	1
Fan2-LSB	A	Fan2-MSB	A	PEC	No-Ack	P

Read input string (0xD4): Reads back the input voltage and input power consumed by the rectifier.

1	7	1	1	8
S	Slave address	Wr	A	Command Code 0xDC

1	1	7	1	1
A	Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = 4	A	Voltage - LSB	A	Voltage - MSB	A

8	1	8	1	8	1	1
Power - LSB	A	Power - MSB	A	PEC	No-Ack	P

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Read_firmware_rev [0 x D5]: Reads back the firmware revision of all three µC in the rectifier.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDD	A

1	1	7	1	1	8	1
A	Sr	Slave Address	Rd	A	Byte Count = 6	A

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
i2c major rev	A	i2c revision	A	PEC	No-ack	P

Read_run_timer [0 x D6]: This command reads back the recorded operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 3	A

8	1	8	1	8	1
Time - LSB	A	Time	A	Time - MSB	A

8	1	1
PEC	No-ack	P

EEPROM record (0xD9): The µC contains 128 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xD9	A

8	1	8	1
Start location	A	Byte count	A

8	1	8	1
first_byte	A	.....	last - byte	A

8	1	1
PEC	A	P

To read contents from the EEPROM section

1	7	1	1	8	1
S	Slave address	Wr	A	Command 0xD9	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1		8	1
Byte 1	A	.....	Byte ≤ 32	A

8	1	1
PEC	No-ack	P

Test Function (0xDF)

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	Service LED	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

LEDS test ON: Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

LEDS test OFF: Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

Service LED ON: Requests the rectifier to ***flash***-ON the Service (ok-to-remove) LED. The ***flash*** sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

Service LED OFF: Requests the rectifier to turn OFF the Service (ok-to-remove) LED.

OR'ing Test: This command verifies functioning of output OR'ing. At least two paralleled rectifiers are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one rectifier should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

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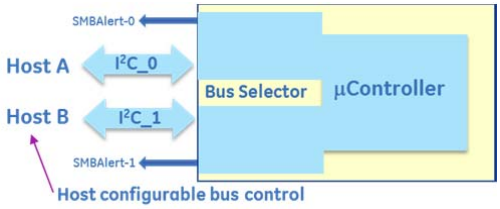
Dual Master Control:

Two independent I²C lines and Alert# signals provide true communications redundancy allowing two independent controllers to sequentially control the rectifier.

A short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time when the bus is idle.



Conceptual representation of the dual I²C bus system.

The Alert# line exciting the rectifier combines the Alert# functions of rectifier control and dual_bus_control.

Status_bus (0xD7): Bus_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The µC may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Bit Position	Flag	Default Value
7	Bus 1 command error	0
6	Bus 1 Alert# enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 Alert# enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	1

Command Execution: The master not in control can issue two commands on the bus, take_over_bus_control and clear_faults

Take_over_Bus_Control(0xD8): This command instructs the internal µC to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I²C selector section of the µC. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Control can be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note; The µC can handle read instructions from both busses simultaneously.

The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

Status Notifications: Once control is transferred both Alert# lines should get asserted by the I²C selector section of the µC. The released 'master' is notified that a STATUS change occurred and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the rectifier. Each master must issue a clear_faults command to clear his Alert# signal.

If the Alert# signal was actually triggered by the rectifier and not the I²C selector section of the µC, then only the 'master' in control can clear the rectifier registers.

Incomplete transmissions should not occur on either bus.

General performance descriptions

Default state: Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled rectifiers during power up. If the overload persists beyond the 20 second delay, the rectifier will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $36V_{DC}$ the Output LED will continue blinking.
When output voltage is < $36V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Restart after a latchoff: **PMBus™** fault_response commands can be configured to direct the rectifier to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON**.**
2. The unit may be commanded to restart via i2c through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart.**

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Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Auto_restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

Fault Management

The rectifier recognizes that certain transitionary states can occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

The rectifier differentiates between **internal faults** that are within the rectifier and **external faults** that the rectifier protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A **state_change** is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a **state_change**;

- Initial power-up of the system when AC gets turned ON . This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each rectifier to reset the system_interrupt.
- Any changes in the bit pattern of either the PMBus standard STATUS or the mfr_specific STATUS registers should trigger the Alert# signal.

Hot plug procedures

Careful system control is recommended when hot plugging a rectifier into a live system. It takes about 15 seconds for a rectifier to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple rectifiers may respond to specific instructions because the address of the hot plugged rectifier always defaults to xxxx000 (depending on which device is being addressed within the rectifier) until the rectifier configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which rectifier is to be removed. The controller turns the service LED ON, thus informing the installer that the identified rectifier can be removed from the system. The system controller should then poll the rectifier_present signal to verify when the rectifier is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the rectifier. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the rectifier is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same rectifier. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the rectifier out of service.

Information only alarms: The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- V_{out} out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery

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- Stby out of limits
- Communication errors

Remote upgrade

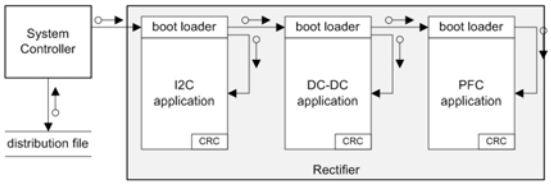
This section describes at a high-level the recommended re-programming process for the three internal micro controllers inside the rectifier when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by GE Critical Power for controller based systems positioned primarily for the telecommunications industry. GE Critical Power will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

For some customers internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from GE Critical Power. This kit contains a turn-key package with the re-program firmware.

Remote upgrade

Conceptual Description: The rectifier contains three independent µControllers. The boost (PFC) section is controlled by the primary µController. The secondary DC-DC converter is controlled by the secondary µController, and I²C communications are being handled by the I²C Interface µController.



Each of the µControllers contains a **boot loader** section and an **application** section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the rectifier.

The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

The Upgrade Package: This package contains the following files;

- **Manifest.txt** - The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary. This file contains the version number and the compatibility code of the upgraded program for each of the three processors

- **Program.bin** - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file
  CP3x00AC54TEZ.zip
- Unzipping the contents shows the following files
  CP3x00AC54TEZ.pfc.bin
  CP3x00AC54TEZ.sec.bin
  manifest.txt
- Opening manifest.txt shows the following
  # Upgrade manifest file
  # Targets: CP3x00AC54TEZ PFC and SEC
  # Date: Tue 01/14/2014 14:25:09.37
  # Notes:
- Program contents
  >p, CP3x00AC54TE _P01, CP3x00AC54TEZ _PFC.bin,1.18
  >s, CP3x00AC54TE _S01, CP3x00AC54TEZ _SEC.bin,1.1
  compatibility code, new program, revision number

Upgrade Status Indication: The FAULT LED is utilized for indicating the status of the re-programming process.

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or programming in progress
Fault	ON	Erase or re-program failed

Wink: 0.25 seconds ON, 0.75 seconds OFF
Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

Upgrade procedure

1. Initialization: To execute the re-programming/upgrade in the system, the rectifier to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the rectifier is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation.

   Note: Make sure that sufficient power is provided by the remaining on-line rectifiers so that system functionality is not jeopardized.
2. Unzip the distribution file
3. Unlock upgrade execution protection by issuing the command below;

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Password(0xE0): This command unlocks the upgrade commands feature of the rectifier by sending the characters 'UPGD'.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE0	A	Byte count - 4	A

8	1		8	1	8	1	1
Byte 0 - U	A	.....	Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

Target list(0xE1) : This command returns the upgradable processors within the rectifier. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd – 0xE1	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count - n	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte n	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the rectifier compatibility code of the target processor.

Compatibility code (0xE2): This read command consists of up to 16 characters defining the hardware configuration:

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 16	A	Byte 0	A

	8	1	8	1	1
.....	Byte 15	A	PEC	No-Ack	P

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

6. Check the software revision number of the target processor in the rectifier and compare it to the revision in the upgrade. If the revision numbers are the same, or the rectifier has a higher revision number then no upgrade is required for the target processor.

Software revision(0xE3): This command returns the software revision of the target.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE3	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count=7	A	Major revision	A

8	1	8	1	8	1	8	1
Minor revision	A	month	A	day	A	year[24]	A

8	1	8	1	8	1	1
hrs	A	min	A	PEC	No-Ack	P

7. Verify the capability of each processor

Memory capability (0xE4): Provides the specifics of the capability of the device to be reprogrammed

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count=7	A	Max bytes	A

8	1	8	1	8	1	8	1
ET-LSB	A	ET-MSB	A	BT-LSB	A	BT-MSB	A

8	1	8	1	8	1	1
App_CRC_LSB	A	App_CRC_MSB	A	PEC	No-Ack	P

Where the fields definition are shown as below:

Max Bytes	Maximum number of bytes in a data packet
ET	Erase time for entire application space (in mS)
BT	Data packet write execution time (uS)
APP_CRC	Application CRC-16 – returns the application CRC-16 calculation. Reading these register values, if the application upload CRC-16 calculation returns an invalid, provides the mismatch information to the host program. (See application status(0xE5) command)

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

[24] Last two digits

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8. **Application status (0xE5):** Returns the Boot Loader's present status

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE5	A	Target-x	A

1	8		1	8	1	8	1	1
Sr	Slave addr	Rd	A	Status	A	PEC	No-Ack	P

Status bits:

0x00	Processor is available	0x10	Reserved
0x01	Application erased	0x20	Reserved
0x02	CRC-16 invalid	0x40	Manages downstream µC
0x04	Sequence out of order		
0x08	Address out of range	0x80	In boot loader

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

9. Issue a Boot Loader command with the *enter boot block* instruction

Boot loader (0xE6): This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

1	7	7	7	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE6	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

Data:

1=enter boot block (software reboot)
2=erase
3=done
4=exit[25] boot block (watchdog reboot)

Note: The target µC field is ignored for enter and exit commands. During this process if the output of the rectifier was not turned OFF the boot loader will turn OFF the output

10. Erase and program each µC using the Boot Loader command, starting with the PFC.

11. Wait at least 1 second after issuing en *erase* command to allow the µC to complete its task.

12. Use command 0xE5 to verify that the PFC µC is erased. The returned status byte should be 0x81.

13. Use the Data Transfer command to update the application of the target µC.

Data transfer (0xE7): The process starts with uploading data packets with the first sequence number (0x0000).

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE7	A	Target-x	A

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count = n	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte n-1	A	PEC	A	P

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE4	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 3	A

1	8	8	1	8	1	8	1	1
Seq-LSB	A	Seq-MSB	A	Status	A	PEC	No-Ack	P

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

14. Execute a Boot loader command to tell the PFC µC that the transfer is done.

    At the completion signal, the PFC µC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

    Wait for at least 1 second to allow time for the PFC µC to calculate the error checking value.

15. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.

16. Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC µC will transfer to the uploaded application code.

17. Wait for at least 1 second.

[25] The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

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18. Use command 0xE1 to verify that the PFC µC is now in the application code. The returned status data bte should be 0x00.

19. Repeat the program upgrade for the Secondary and I²C µC's, if included in the upgrade package.

Product comcode

Although the comcode number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

Product comcode (0xE8):

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE8	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 11	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte 10	A	PEC	No-Ack	P

Error handling: The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending rectifier from service.

Black box

Contents of the black box and more detailed information about the specifics of the feature are described in a separate document. The intent here is to provide a high level summary This feature includes the following;

1. A rolling event Recorder
2. Operational Use Statistics

The rolling event recorder

The purpose of the black box is to provide operational statistics as well as fault retention for diagnostics following either recoverable or non-recoverable fault events. Sufficient memory exists to store up to 5 time-stamped snapshot records (pages) that include the state of the status and alarm registers and numerous internal measurement points within the power supply. Each record is stored into nonvolatile memory at the time when a black box trigger event occurs. Once five records are stored, additional records over-write the oldest record.

The memory locations will be cleared, when the product is shipped from the GE factory.

Operational use statistics

This feature of the black box includes information on the repetition and duration of certain events in order to understand the long-term operational state of the power supply. The events are placed into defined buckets for further analysis. For example; the power supply records how long was the output current provided in certain load ranges.

Accessing the event records

The event records are accessed by uploading the entire contents of the black box of the power supply into a folder assigned by the user. Within the I²C protocol this upload is accomplished by the upload_black_box (0xF0) command described below. GE provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

Upload black box(0xF0): This command executes the upload from the power supply to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the power supply to gather the required data from the secondary DSP controller.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd – 0xF0	A

8	1	8	1
Start address - msb	A	Start address - lsb	A

8	1	
Length = N (≤ 32)	A	..... delay 100ms

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Length ≤ 32	A	Byte 0	A

.....	8	1	8	1	1
	Byte N-1	A	PEC	No-Ack	P

If a transmission error occurs, or if the uC did not receive the data from the DSP, the uC may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by rev 1.3 of the GE Interface Adapter is 32 x 64 comprising 2048 bytes of data.

Start Address	0 ..... Byte 31
0000h	
0020h	
0040h	
.	
.	
.	
.	
.	
.	
.	
.	
07E0h	

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CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277 Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

Table 1: Alarm and LED state summary

	Rectifier LED State					Monitoring Signals			
Condition	AC OK Green	DC OK Green	Service Amber	Fault Red		Fault	OTW	PFW	Module Present
OK	1	1	0	0		HI	HI	HI	LO
Thermal Alarm (5C before shutdown)	1	1	1	0		HI	LO	HI	LO
Thermal Shutdown	1	0	1	1		LO	LO	LO	LO
Defective Fan	1	?[26]	0	1		LO	HI	LO	LO
Blown AC Fuse in Unit	1	0	0	1		LO	HI	LO	LO
AC Present but not within limits	Blinks	0	0	0		HI	HI	LO	LO
AC not present[1]	0	0	0	0		HI	HI	LO	LO
Boost Stage Failure	1	0	0	1		LO	HI	LO	LO
Over Voltage Latched Shutdown	1	0	0	1		LO	HI	LO	LO
Over Current	1	Blinks	0	0		HI	HI	Pulsing[4]	LO
Non-catastrophic Internal Failure[2]	1	1	0	1		LO	HI	HI	LO
Standby (remote)	1	0	0	0		HI	HI	LO	LO
Service Request (PMBus mode)	1	1	Blinks	0		HI	HI	HI	LO
Communications Fault (RS485 mode)	1	1	0	Blinks		HI	HI	HI	LO

[1] This signal is correct if the rectifier is back biased from other rectifiers in the shelf .
[2] Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.
[3] Signal transition from HI to LO is output load dependent
[4] Pulsing at a duty cycle of 1ms as long as the unit is in overload.

Table 2: Signal Definitions

All hardware alarm signals (Fault#, PFW#, OTW#) are open drain FETs. These signals need to be pulled HI to either 3.3V or 5V. Maximum sink current 5mA. An active LO signal (< $0.4V_{DC}$) state. All signals are referenced to Logic_GRD unless otherwise stated.

Function	Label	Type	Description
Output control	ON/OFF	Input	If shorted to Logic_GRD main output is ON in Analog or PMBus mode.
Power Fail Warning	PFW#	Output	An open drain FET; Changes to LO ≅ 5msec before the output decays below $40V_{DC}$.
I^2C Interrupt	Alert#_0/Alert#_1	Output	This signal is pulled to 3.3V via a 10kΩ resistor. Active LO.
Rectifier Fault	Fault#	Output	An open drain FET; normally HI, changes to LO.
Module Present	MOD_PRES	Output	Short pin, see Status and Control description for further information on this signal.
Interlock	Interlock	Input	Short pin, controls main output during hot-insertion and extraction. Ref: Vout (-)
Protocol select	Protocol	Input	Selects operational mode. Ref: Vout (-). No-connect PMBus, 10kΩ - RS485
Margining	Vprog	Input	Changes the set point of the main output.
Over-Temperature Warning	OTW#	Output	Open drain FET; normally HI, changes to LO 5°C prior to thermal shutdown.
i2c address	Unit_ID	Input	Voltage level selecting the A3 - A0 bits of the address byte
i2c address	Rack_ID	Input	Voltage level selecting the A3 – A0 bits of the address byte
Back bias	8V_INT	Bi-direct	Used to back bias the DSP from operating Rectifiers. Ref: Vout (-).
Standby power	5VA	Output	5V at 2A provided for external use
Current Share	Ishare	Bi-direct	A single wire active-current-share interconnect between rectifiers Ref: Vout (-).
I^2C Line 0	SCL_0	Input	PMBus line 0.
I^2C Line 0	SDA_0	Bi-direct	PMBus line 0.
I^2C Line 1	SCL_1	Input	PMBus line 1.
I^2C Line 1	SDA_1	Bi-direct	PMBus line 1.
RS485 Line	RS_485+	Bi-direct	RS485 line +
RS485 Line	RS_485-	Bi-direct	RS485 line -

[26] A single fan fault may not cause a shutdown. Shutdown is controlled by internal unit temperatures. A double fan fault causes an immediate shutdown.

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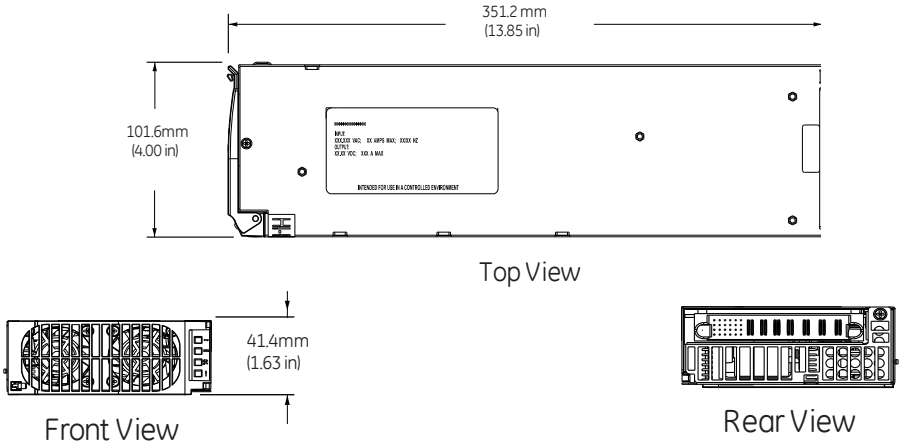
CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

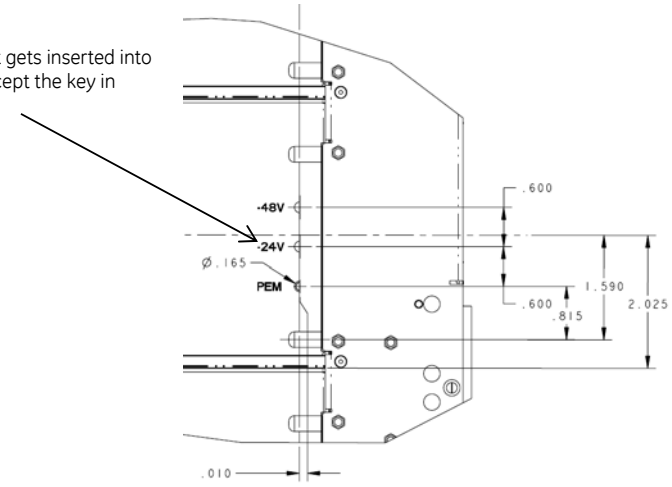
Mechanical Outline

Dimensions



Shelf insertion keying

The cover of the rectifier is notched to ensure that it gets inserted into the correct shelf. The notch has to be located to accept the key in position 2 (-24V location in original design).



Front Panel LEDs

	Analog Mode	I²C Mode	RS485 Mode
☐ ~	←	**ON:** Input ok **Blinking:** Input out of limits	→
☐ ⎓	←	**ON:** Output ok **Blinking:** Overload	→
☐ 🛠	**ON:** Over-temperature Warning	**ON:** Over-temperature Warning **Blinking:** Service	**ON:** Over-temperature Warning
☐ !	← **ON:** Fault →		**ON:** Fault **Blinking:** Not communicating

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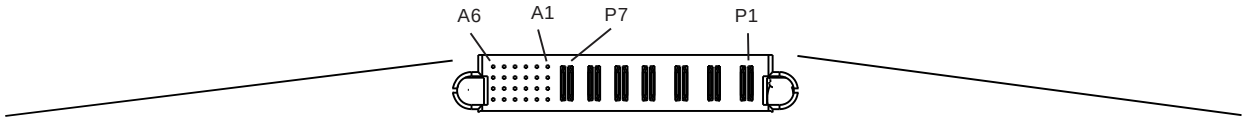
CP3000/3500AC54TE CPL High Efficiency Rectifier

Input: 100-120/220-277 Vac; Default Output: ±54 Vdc @ 3500W; 5 Vdc @ 10W

Output Connector

TE: 3-6450832-8, or **FCI:** 10106262-7006001LF

Mating Connector: right angle PWB mate – all pins: **TE** – 1-6450872-6, **FCI** – 10106264-7006001LF;
right angle PWB mate except pass-thru input power: **TE** – 6450874-3, **FCI** – 10106265-70CB001LF



	SIGNAL						OUTPUT POWER				INPUT POWER		
	6	5	4	3	2	1	P7	P6	P5	P4	P3	P2	P1
A	SCL_0	MOD_PRES	PFW#	LOGIC_GRD	RS_485+	Slot_ID							
B	SCL_1	OTW#	Alert#_0	Alert#_1	RS_485-	8V_INT	V_OUT	V_OUT	V_OUT	V_OUT	EARTH	LINE-2	LINE-1
C	SDA_0	Vprog	ON/OFF	Rack_ID	Ishare	Protocol	(-)	(+)	(+)	(-)	(GND)	(Neutral)	(HOT)
D	SDA_1	Fault#	5VA	Unit_ID	Interlock	Shelf_ID							

Note: Connector is viewed from the rear positioned inside the rectifier

Signal pins columns 1 and 2 are referenced to V_OUT (–) . Slot_ID and Shelf_ID are used only with RS485 communications.

Signal pins columns 3 through 6 are referenced to Logic GRD

	Last to make-first to break shortest pin
Earth	First make-last to break longest pin implemented in the mating connector

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Appendix

Bus transfer reporting

operation	Alert#0	Alert#1	status_bus	status_word	status_cml	
i2c1-command sent, not in control	0	1	0xC1	0x0000	0x00	
i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
i2c1 takes over control	1	1	0x74	event1	0x00	
i2c1 read system status	1	1	0x74	event1	0x00	controller needs to read status before clearing the registers.
i2c1 issues a clear_faults	0	0	0x14	0x0000	0x00	Assuming that the event has cleared
i2c0 reads system status	0	0	0x14	0x0000	0x00	fault
i2c0 issues clear faults	0	0	0x10	0x0000	0x00	
i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
i2c0 issues clear faults	0	0	0x01	0x0000	0x00	Assuming that the event has cleared
i2c1 in control	0	0	0x10	0x0000	0x00	
i2c0 takes over control	1	1	0x47	0x0000	0x00	
i2c0 issues a clear_faults	0	1	0x41	0x0000	0x00	
i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
i2c1 in control	0	0	0x10	0x0000	0x00	
i2c0 issues a command	1	0	0x1C	0x0000	0x00	the command is rejected because i2c0 is not in control
i2c0 issues a clear_faults	0	0	0x10	0x0000	0x00	
i2c1 issues a bad command	0	1	0x10	0x0002	0x80	
i2c1 issues a clear_faults	0	0	0x10	0x0000	0x00	

Latched status states until cleared

The following bits are sticky until cleared by the customer

Or'ing test failed or passed: I cannot see how it could be otherwise. The customer needs to delete the information (clear_faults) thus indicating that he received the information.

Restarted_ok: this bit has been removed from the requirements. PMBus latched states replace this bit.

Shutdown: must be sticky – it tells the customer that the power supply output has been turned OFF

OV, UV, OC, fan, input, unknown warnings & faults, CML Errors, Internal or External Fault: must be sticky

OC and OT response registers are in their own confined state. The only way these should change is by commanding the change by the controller. So theoretically they are sticky because a clear_faults should never change them.

The way to look at this is, all fault information is sticky (if the fault still persists after a clear_faults has been issued then the fault state will reassert), all operational state information is not sticky.

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Ordering Information

Please contact your GE Sales Representative for pricing, availability and optional features.

Table 4: Device Codes

Item	Description	Comcode
CP3000AC54TEZ	3000W output power capacity, 5Vdc @ 2A, RoHS 6/6,	150033916
CP3000AC54TECZ	3000W output power capacity, 5Vdc @ 2A, RoHS 6/6, Improved input measurement	150041904
CP3500AC54TEZ	3500W output power capacity, 5Vdc @ 2A, RoHS 6/6,	150030396
CP3500AC54TECZ	3500W output power capacity, 5Vdc @ 2A, RoHS 6/6, Improved input measurement	150041901

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